Application of TECs to Thermal Management of 3D ICs

Introduction

The advent of vertical chip integration, in recent years, has allowed 3D chips to overcome issues such as delay, bandwidth limitation and power consumption in interconnects, which occurs in traditional integrated circuits. By stacking the chips, the footprint of an IC has been drastically reduced; also, the length of the interconnecting wires has been considerably shortened by using vertical vias.

From the thermal perspective, 3D stacked chips pose different challenges than what has been experienced in 2D packaging. For example, the heat dissipation of 3D ICs is highly non-uniform and multidirectional, due to the intrinsic chip architecture and the available real estate. When cooling at sub-ambient temperatures is necessary, as may be the case for future applications, the small footprint of a 3D chip becomes an impediment to deploying a cooling solution. Additionally, precision temperature control becomes difficult, since the surface to be controlled may be buried deep in the 3D stack. In response to cooling concerns about 3D ICs, this article presents a review of methods available for cooling 3D ICs to sub ambient temperatures using TECs.

Multi-Dimensional Heat Transfer System (MHTS)

A novel method to address thermal issues in 3D ICs has been proposed by Phan and Agonafer [1].

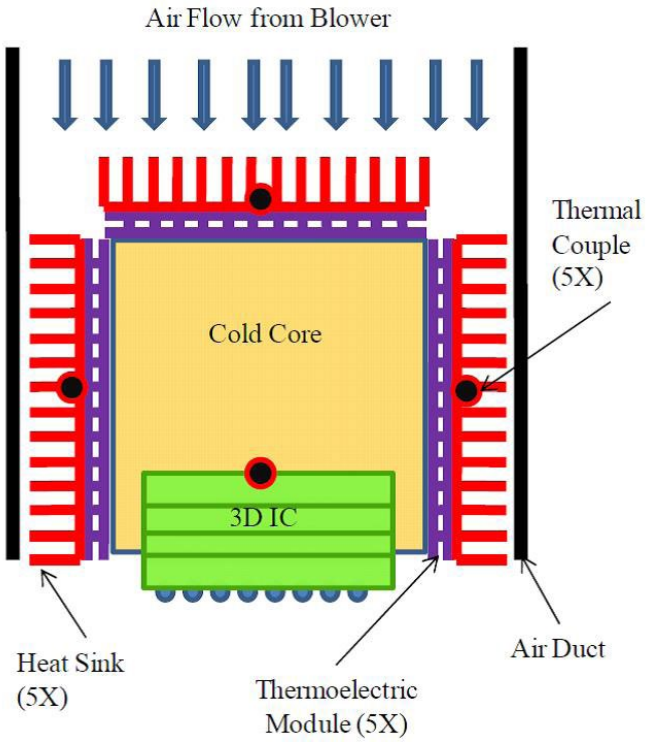

Figure 1. Multi-Dimensional Heat Transfer Module in its Simplest Form [1]

The idea is to cool a 3D chip utilizing the vertical space around the chip and only the available real estate on the PCB. In its simplest form (Figure 1), it is comprised of a cubical center core acting as an extended fin, cooled by 5 thermoelectric modules. The center core is made of a thermally conductive material (copper, carbon graphite, aluminum). Each TEC module has a heat sink attached to it.

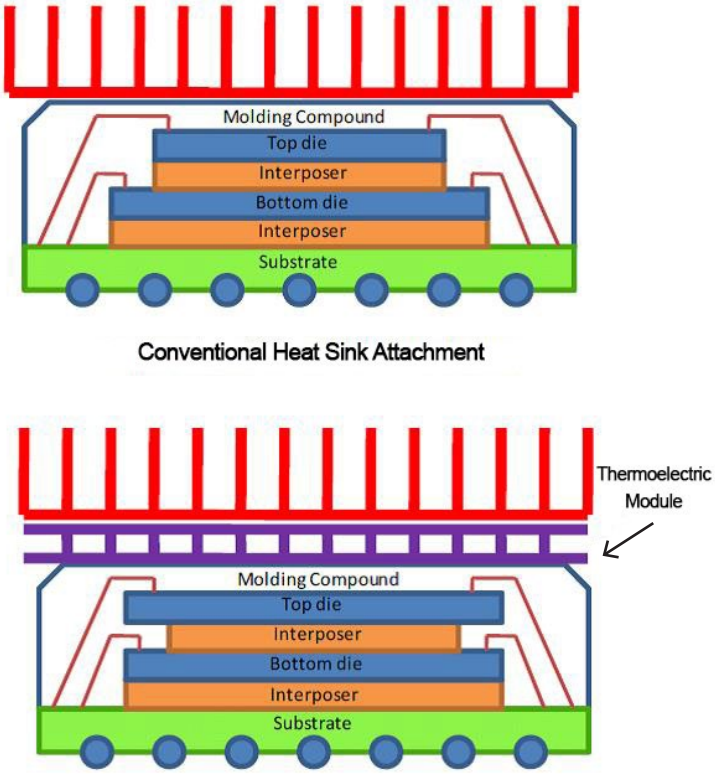

Figure 2. Conventional Cooling Methods of a 3D IC [1]

To test the effectiveness of this proposed cooling method, it was compared against two conventional methods: a heat sink without a TEC and heat sink with one TEC module (Figure 2). For the first case, the air flow rate was varied between 0.0086 and 0.0127 m^3/s. In the second case, the airflow rate varied between 0.009 and 0.017 m^3/s and the power input to the TEC was in the range of 5 to 95 W. The two cases were used as benchmarks for the results obtained with MHTS (the third case). For all cases tested, identical heater and heat sink sizes were used in order to emphasize the real estate limitation.

All three cases were tested in the airflow chamber shown in Figure 3. Thermocouples were inserted into the heat sink bases as well as inside the heater that simulated the processor (chip). The chip temperature was recorded for each airflow rate. The ambient temperature and relative humidity were 20 °C and 50%, respectively.

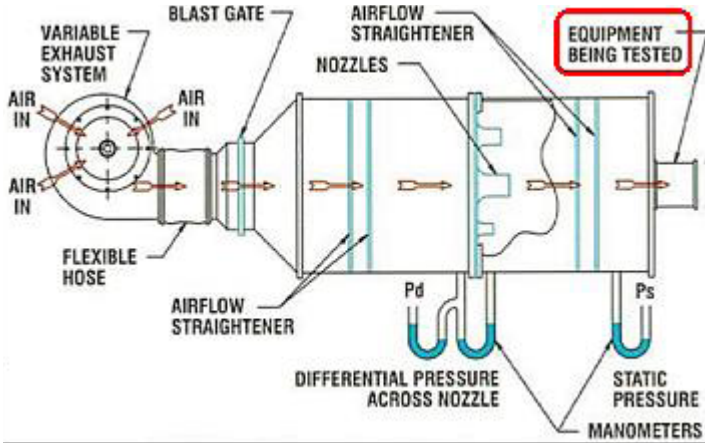

Figure 3. Air Flow Bench Test Set Up [1]

Test Results

For the first case tested (heat sink only), the chip temperature ranged from 34.5 °C to 32.5 °C, as illustrated in Figure 4. It is possible to reduce the chip temperature further, but at the expense of above allowable limit of acoustic noise. For this case, sub-ambient cooling is not possible.

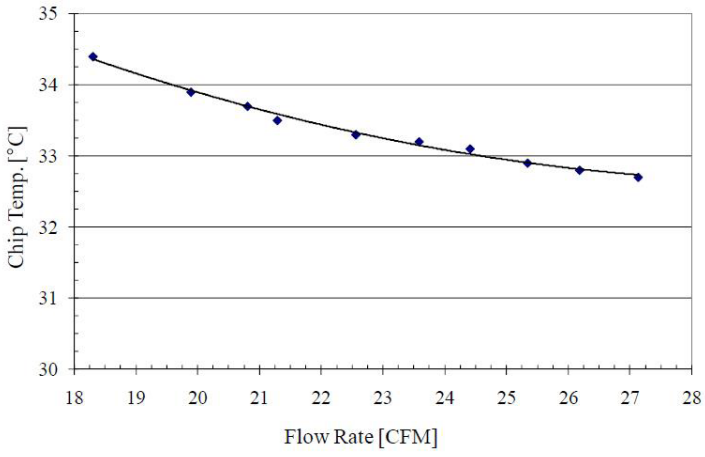

Figure 4. Chip Temperature as a Function of Airflow (Heat Sink Only) [1]

The second case, with one TEC module sandwiched between the chip and the heat sink, produced results shown in Figure 5. The chip temperatures were higher than in the previous case, with the

lowest being 52.5 °C for 0.0168 m³/s airflow and 35 W input power to the TEC. This is due to the fact that the heat sink was unable to cool the processor and the TEC, since the real estate available for the heat sink on the motherboard was restricted. Such a case illustrates that using TECs is not readily beneficial; if a heat sink is able to accommodate the extra power generated by the TEC, the TEC produces adverse effects. The third case (MHTS) produced the desired results (Figure 6). The chip temperature descended below ambient for all the airflow rates tested in a certain TEC input power range. At an airflow of 0.0104 m³/s and with 90 W of input power to the TEC, the chip temperature was 13 °C.

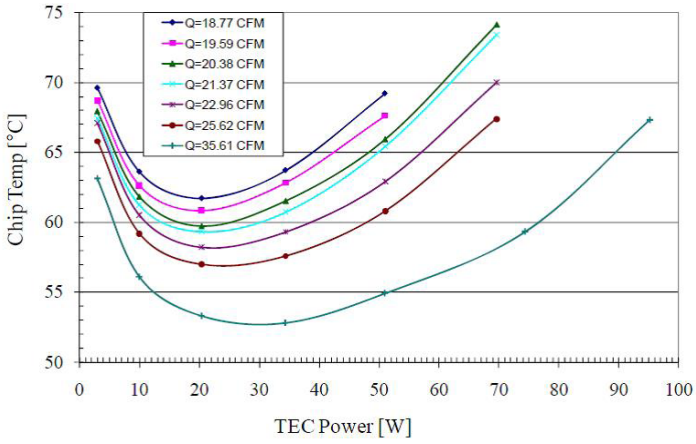

Figure 5. Chip Temperature as a Function of Airflow and TEM Input Power (1D TEC) [1]

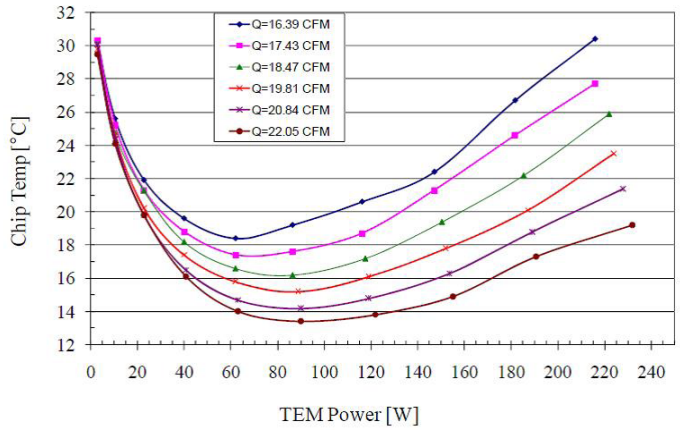

Figure 6. Chip Temperature as a Function of Airflow and TEM Input Power (MHTS) [1]

3D ICs with embedded TECs

Recently, IBM researchers proposed 3D stacks with TEC inter-layers [2]. Such a solution employs thermal through silicon vias (TSVs), to bring power to the TEC (102c) as well as to internally conduct the heat from the hot side of the TEC to the heat sink (Figure 7). The TSVs are filled with high thermal conductivity metals. Coupling layers (132 a and b) link the TEC with the lower and upper chips. These layers are made of dielectric materials with good thermal conductivity, such as CVD diamond or silicon carbide (SiC). This chip architecture allows reaching very low internal temperatures for certain regions of interest (hot spots). However, in a practical implementation, such a solution must be coupled with adequate cooling at the external chip surfaces, since the generated heat will exceed that produced by a regular 3D IC.

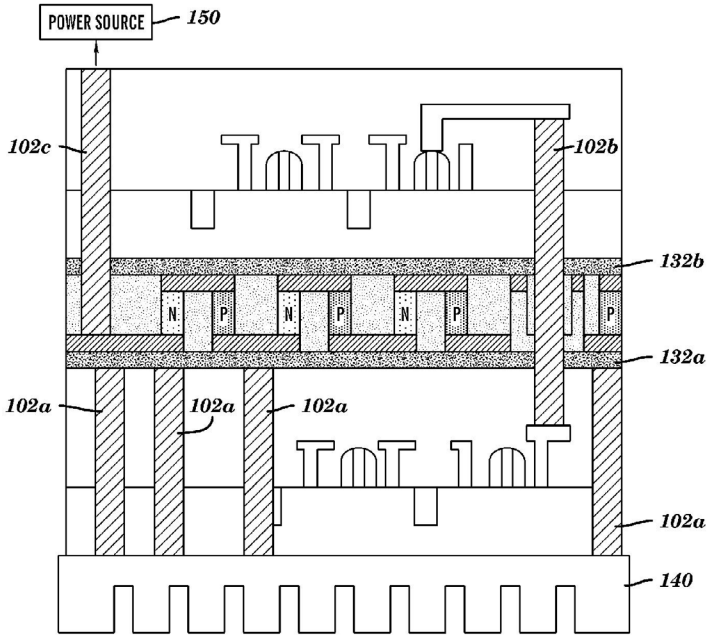

Figure 7. 3D IC Architecture with Embedded TEC Layer [2]

Conclusions

Two TEC based cooling methods for 3D ICs have been presented. It has been shown that sub-ambient chip temperatures can be achieved without exceeding the PCB real estate allocated for thermal management. However, several observations are noteworthy. For the MHTS method, the tests were not done with an actual fan or blower; rather, any airflow rate needed was assumed to be available. In reality, this may not be the case. Also, the solution involved multiple TECs and heat sinks, which may pose reliability problems in an actual implementation.

For the 3D ICs with internally built TEC layer, the chip structure becomes complex and difficult to manufacture. Also, adequate cooling at the external chip surfaces must exist, since the generated heat will exceed that produced by a regular 3D IC.

References:

1. **Phan, H. and Agonafer, D., " Experimental Analysis Model of an Active Cooling Method for 3D-ICs Utilizing a Multidimensional Configured Thermoelectric", 26th IEEE SEMI-THERM Symposium, 2010.**

2. **US Patent 8,030,113 B2, Oct.4 2011.**

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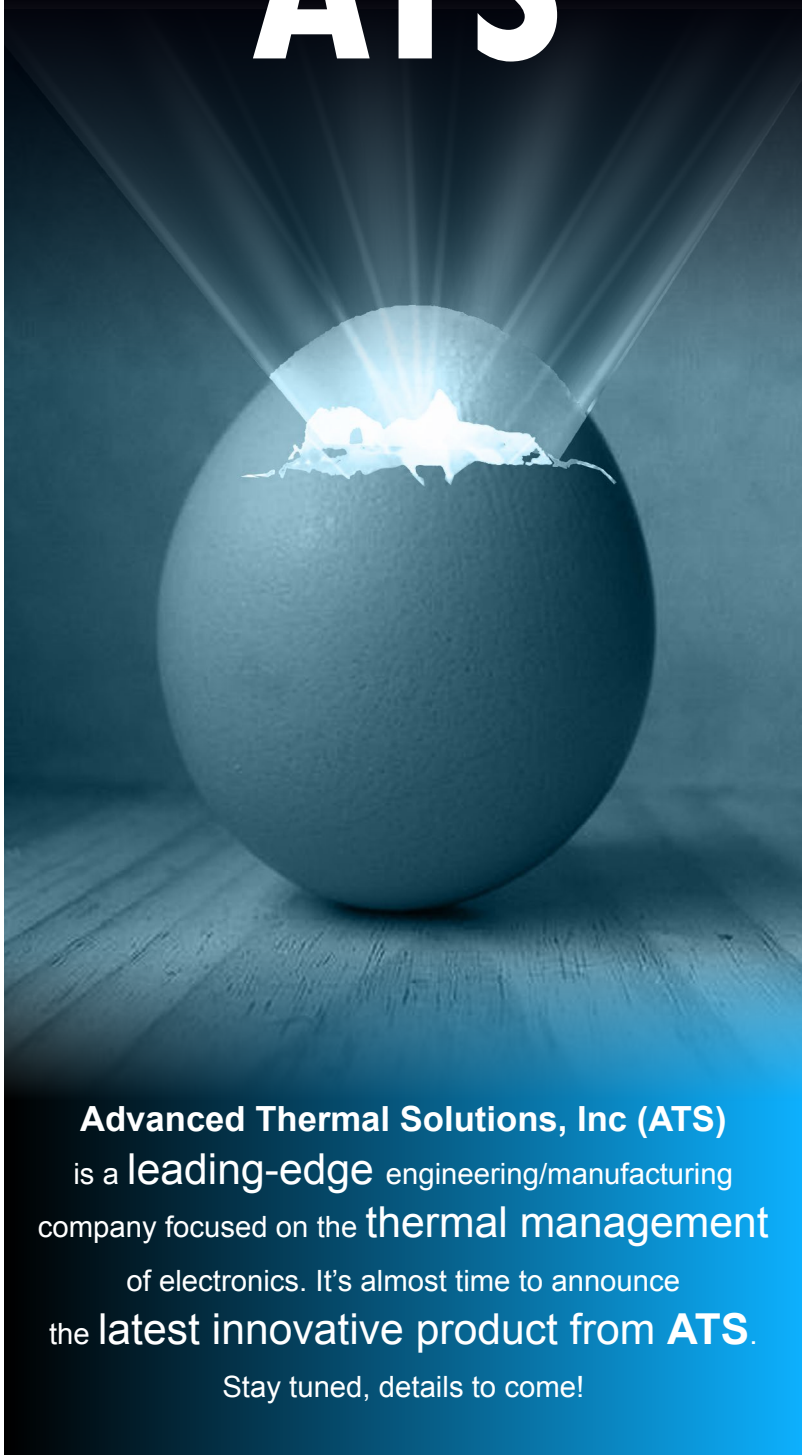

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